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## (54) Optical calibration test standard for surface inspection systems.


(57) This universally applicable optical calibration standard for surface inspection systems has a plurality of hemispherical pads (16) which simulate the light scattering due to particulate contamination. The hemispherical pads (16) scatter light (10) irrespective of angles of illumination and detection and of rotational orientation, and are fabricated using ball-limiting metallurgical techniques. Any number and sizes of pads (16) can be arranged on a flat, optically reflective substrate (12) and the standard can be repeatedly cleaned, thereby having a long useful life.


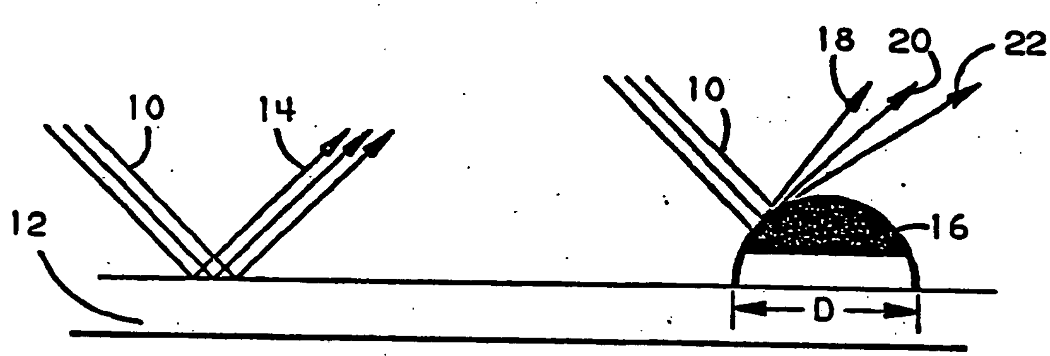


FIG. 1


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# OPTICAL CALIBRATION TEST STANDARD FOR SURFACE INSPECTION SYSTEMS

This invention relates to calibration standards for surface inspection systems.

The need for the calibration of wafer surface inspection systems has been widely recognized by the semiconductor manufacturing industry. These systems are used for the detection, identification, and measurement of the number and sizes of particles on, or in, the surface of semiconductor wafers. The prior absence of a suitable calibration standard has resulted in skepticism regarding the daily performance and reliability of these instruments. In the prior art, there have been several attempts to fabricate a standard using a variety of known features to provide a light-scattering response that is comparable to the levels observed with particulate contamination. These features include the use of polystyrene (latex) spheres, etched pits/holes, raised frustums, and thin wires or fibers.

One of the most prevalent methods of establishing the sensitivity of these systems has been the atomization and deposition of a dilute suspension of monodisperse, polystyrene spheres in a random pattern upon the surface of a semiconductor wafer. Despite the availability, uniformity, and repeatability of these spheres, there are a number of problems associated with this method of calibration. The major limitation is that each sphere must be characterized as to its size and its location on the wafer using optical and/or electron microscopy. This long and tedious procedure is required to distinguish each sphere from either surface contamination, or from clusters of spheres that have agglomerated. The spacing between the spheres must also be considered, because if the spacing between two or more spheres is less than the resolution capabilities of the detector, then the spheres will not be resolved from one another and will be detected as a single, larger sphere. A further limitation is that when the wafer becomes heavily contaminated, it must be discarded because of the difficulty in distinguishing the spheres from the surface contamination.

Due to the numerous problems with using latex spheres, there have been several attempts to fabricate a substrate with an easily recognizable pattern of: either etched pits (or holes) or raised frustums to simulate particulate contamination. Although these standards are permanent and capable of being cleaned of any surface contamination, there are some inherent disadvantages associated with their use. First, unless these features are circular in shape, their scattering responses will change with the orientation of the substrate within the system. Even if the features are circular, the response is still dependent upon the illumination and detection geometries of the instrument, since these features scatter light in an anisotropic manner. Therefore, these prior calibration standards have failed to have universal application, and can only serve as references for maintaining the repeatability of a specific type of wafer surface inspection system.

It is highly desirable to have a universal calibration standard which can be used not only as a reference for maintaining the repeatability of a specific type of wafer surface inspection system, but also to have universal application such that different types of wafer surface inspection systems can be readily compared and/or set at a common sensitivity.

Therefore, it is the object of this invention to provide an improved optical calibration standard which can be used on all types of optical inspection equipment.

It is a further object to provide an improved calibration standard that is independent of angles of illumination and detection and of rotational orientation.

It is an additional object to provide an optical calibra tion standard that can be regularly cleaned and reused.

It is a related object of this invention to provide a improved method for making an optical calibration standard

In accordance with these objects, an improved unive sal calibration standard includes a patterned array of hem spherical solder dots, which are first evaporated onto th surface of a semiconductor wafer in the form of circul frustums, and then melted and cooled so that they form in uniform hemispheres. The reflectivity of such an array hemispherical dots is uniform with respect to the angle illumination and detection of the measuring instrument ar also independent of the rotational orientation of the calibra tion standard.

The foregoing and other advantages of the inventio will be more fully understood with reference to the descrip tion of an embodiment and the drawing wherein:

Fig. 1 shows diagrammatically a hemispherical pad on substrate;

Figs. 2a-c illustrate three methods of fabricating the unive sal calibration standard of the invention;

Fig. 3 shows a semiconductor wafer with a plurality rectilinear arrays of hemispherical pads.

Referring to Fig. 1, conventional surface inspectio systems use either bright-field and/or dark-field inspectio techniques. In both cases light 10 striking the surface of substrate 12 is reflected in a specular manner as shown light beam 14. With the placement of a hemispherical pa 16 to simulate particulate contamination in the path of lig 10, scattering in diffuse directions 18, 20 and 22 occurs.

The substrate 12 for the calibration standard idea should have a highly reflective and exceptionally clea surface such that light will easily be reflected with a mi mum of stray light scattering. A semiconductor wafer chosen as the substrate in the preferred embodiment. Th hemispherical pad 16 results from reflowing a circular met frustum 24 (Figs. 2a-c) at an elevated temperature. Th hemispherical shape results from the interaction betwe the surface tension of a solder layer 26 and the adhesi forces between the solder 26 and underlying metallic laye 28. A primary consideration in producing hemispheric pads is the melting point and bonding properties of th solder layer 26. The solder should be relatively low-meltin be capable of undergoing reflow, and be non-bonding to th selected substrate 12. Typical metals that have been us in other reflow applications include solder alloys of lead, ti gold, indium, and/or bismuth. Pure tin is the primary choi for solder layer 26 since it is slightly harder and mo durable than most lead alloys, and forms a thin, protectiv surface layer of metal oxide when in contact with th atmosphere. An even better choice would be the use pure gold, or a lower melting eutectic gold-tin alloy, becau of its excellent resistance to oxidation.

The underlying metallic layers 28, known as ba limiting metallurgy (BLM), serve as a bonding interfa between the solder layer 26 and the surface of the su strate 12. The BLM 28 is comprised of thin layers 30, : and 34 of metals which define the base diameter (D) of th hemispherical pad. A number of metals can be used for th composition of the BLM 28. A single layer of nickel com prising layers 30 and 32 will adhere to both a silic

substrate 12 and to the solder layer 26. As an alternative, chromium or titanium, used in layer 30, will adhere to the silicon substrate 12. An additional layer of copper 32, will adhere to the chromium or titanium layer 30 and form an intermetallic bond with the solder layer 26. After the deposition of the nickel or copper layer 32, a thin layer of gold 34 is deposited to provide a passivation layer to prevent oxidation and subsequent poor adhesion between layer 32 and the solder layer 26. After reflowing the circular frustum 24 at an elevated temperature in a hydrogen reflow furnace, a hemispherical solder pad 16 (Fig. 1), is produced, with the gold layer 34 being incorporated into the solder pad 26.

Referring to Fig. 2a, a resist lift-off masking technique is illustrated. Before the deposition of the metal layers 26, 30, 32, 34, a lift-off layer of polysulfone 36, a barrier layer 38, and a resist layer 40 are first applied, in succession on substrate 12. Pattern definition is then done using conventional lithographic techniques (optical, electron beam, x-ray, etc.) with the corresponding resist 40. The lift-off structure is formed by reactive ion etching of the barrier layer 38 (e.g. methyl siloxane resin or silicon nitride) with a carbon tetrafluoride plasma, followed by an oxygen plasma to etch through the lift-off layer 36. Following the evaporation and deposition of the BLM 28 and solder layer 24, the lift-off of the undesired metal layers 26' and 28' is performed with a solvent (e.g. n-methyl-2-pyrrolidone) that dissolves the lift-off layer 36, leaving the metal frustum 24.

As shown in Fig. 2b, the frustum can also be manufactured using a subtractive etch process. The metal layers 30, 32, 34 and 26 are first evaporated and deposited onto substrate 12. After applying a positive (or negative) photoresist layer 40, conventional lithographic techniques are used to expose the resist areas surrounding each intended metal frustum 24. After the removal of the exposed (or unexposed) resist, the unwanted metal surrounding each intended frustum 24 is removed by either wet or dry etching as known in the art.

Alternatively, a metal masking technique can be used instead of resist masking techniques. Referring to Fig. 2c, the BLM 28 and solder layer 26 are evaporated and deposited through a metal (e.g. molybdenum) mask 42. This technique is limited to the fabrication of relatively large hemispherical features greater than approximately 50 µm. With the use of a neutral density (ND) filter, the scattering responses produced by these features can be attenuated to a lower level that corresponds to smaller feature sizes (assuming the scattering responses are linear over the entire range). In addition to producing the same net response produced by smaller features, the background surface contamination would also be reduced, possibly to a level below the detection limits of the inspection system.

The critical parameters that must be controlled in the fabrication processes outlined with reference to Fig. 2 are the following:

Base diameter of the BLM -- D;

Final metal deposition height -- H;

Mask height -- M;

Mask overhang -- W.

The relationship between these variables is given by the equation:

$$\frac{4W^2H^3}{M^2} - \frac{6DWH^2}{M} + 3D^2H - D^3 = 0$$

To ensure adequate coverage of the entire BLM 28 by the hemispherical solder pad 26, it is suggested that the BLM 28 thickness be no greater than approximately one-sixth of the base diameter D of the BLM 28. This translates to roughly equivalent deposition thicknesses for both the BLM 28 and the solder layer 26.

The parameters of major, but less than primary importance, include the size, spacing and arrangement of the features, avoidance of extraneous features, and wafer size. Referring to Fig. 3, there is depicted an arrangement of hemispherical solder pads 16 on the surface of the substrate 12. By using recognizable and patterned (e.g. rectilinear) arrays of features 44, each hemispherical pad 16 can be easily distinguished from low levels of surface contamination. Furthermore, an array has been placed in the center and in each quadrant of the substrate 12 so that the illumination and the detection uniformity of the inspection system can be quickly checked. The spacing between the features is greater than the resolution capabilities of the detector so that each pad can be resolved from one another.

In the embodiment illustrated in Fig. 3, there are three different feature sizes in each array 44. Feature sizes used range from one to 150 µm in diameter. The advantages of using multiple feature sizes on the same substrate is that multiple sensitivities of the detection system are capable of being established, as well as the linearity of the detection system. While only one feature size can be a perfect hemisphere, unless multiple masking and deposition steps are used, feature sizes up to three times the diameter of this perfect hemisphere can be used. The expected error is less than five percent which is well below the typical size resolution and precision of most inspection systems available.

Because of the permanent nature of the features, the calibration standard can be cleaned repeatedly of any surface contamination by conventional wafer cleaning procedures without harming or altering the size or shape of the features, and without otherwise affecting their ability to scatter or reflect light. In order to minimize accumulated surface contamination on the substrate, it would be advantageous to use a conductive substrate such as metal, heavily doped semiconductor wafer, etc. to minimize electrostatic attraction for particulate contamination.

## Claims

1. Optical calibration test standard, characterized by a flat substrate (12) having an optically reflective surface and at least one hemispherical pad (16) attached to said flat, reflective substrate (12).

2. Optical calibration test standard in accordance with claim 1, characterized in that said hemispherical pads (16) are arranged in at least one patterned array (44) on said

substrate (12).

3. Optical calibration test standard in accordance with any one of claims 1-2, characterized in that said flat, optically reflective substrate (12) is metallic and electrically conductive.

4. Optical calibration test standard in accordance with any one of claims 1-2, characterized in that said flat, optically reflective substrate (12) is a semiconductor wafer.

5. Optical calibration test standard in accordance with claim 1, characterized in that said hemispherical pads (16) include a layer of solder (26), the solder being selected from the group consisting of gold, tin, lead, indium and bismuth.

6. Optical calibration standard in accordance with claim 5, characterized in that said hemispherical pads (16) further include a layer of chromium (30).

7. Optical calibration standard in accordance with claim 5, characterized in that said hemispherical pads (16) include a layer of titanium (30).

8. Optical calibration standard in accordance with claim 5, characterized in that said hemispherical pas (16) further include a layer of nickel (30, 32).

9. Optical calibration standard in accordance with any one of claim 1, 6 and 7, characterized in that said hemispherical pads (16) further include a layer of copper (32).

10. Optical calibration standard in accordance with claim 9, characterized in that said hemispherical pads (16) further include a layer of gold (34).

11. Optical calibration test standard in accordance with claim 1, characterized in that of the plurality of hemispherical pads attached to said substrate (12), at least one of said pads (16) has a diameter different from the rest of said pads (16), whereby multiple size sensitivities of said inspection systems can be determined.

12. Optical calibration test standard in accordance with claim 11, characterized in that said hemispherical pads (16) have diameters in the range from one to 150 micrometers.

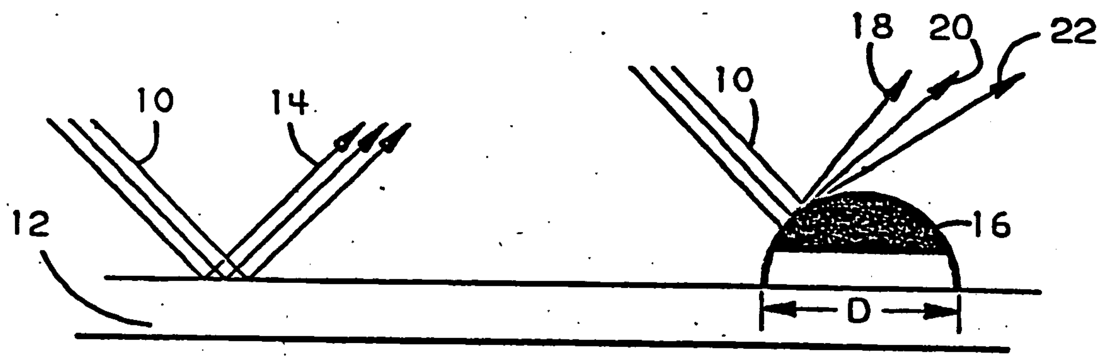


FIG. 1



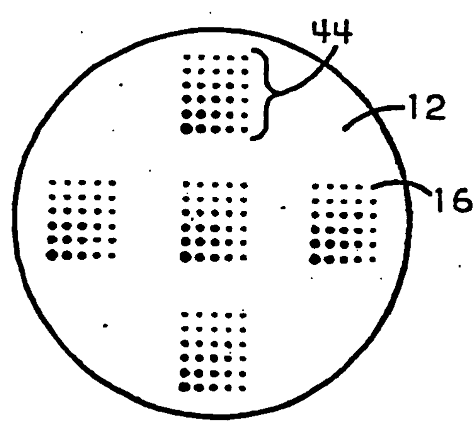


FIG. 3

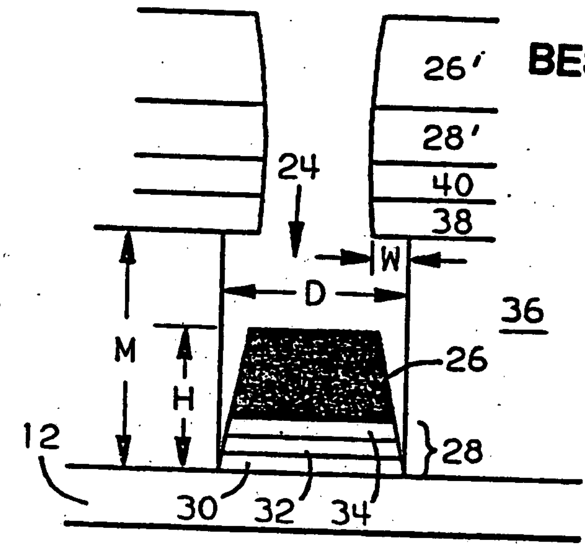


FIG. 2A

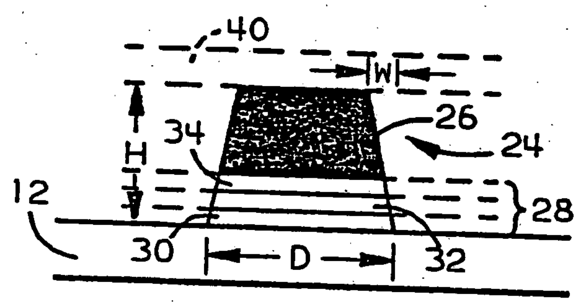


FIG. 2B

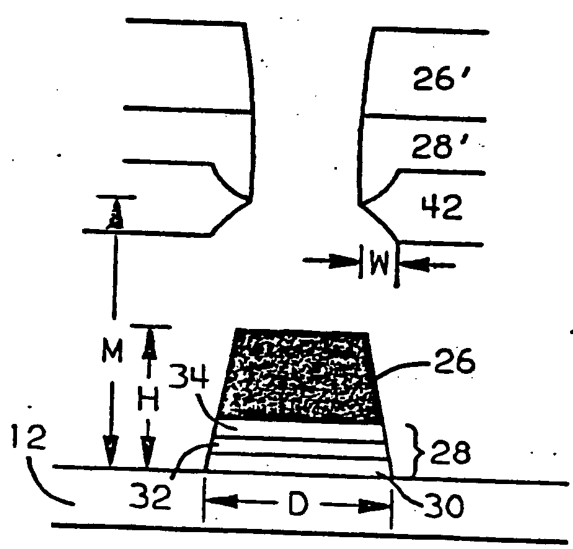


FIG. 2C

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# EUROPEAN SEARCH REPORT

Application number

EP 85112276.2

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int. Cl.4) |
|---|---|---|---|
| X | DE - B2 - 2 522 346 (SIEMENS)<br>* Totality *<br>-- | 1,2,4,5 | H 01 L 21/00<br>G 01 M 11/00 |
| X | DE - B2 - 1 790 173 (SONY)<br>* Claims; column 8, lines 28-40; fig. 15A,A' *<br>-- | 1,2,4 | |
| A | US - A - 4 179 622 (MORITZ)<br>* Summary; fig. 3 *<br>-- | | |
| A | US - A - 4 390 279 (SUWA)<br>* Totality *<br>-- | | |
| A | EP - A1 - 0 040 704 (IBM)<br>* Claims; fig. *<br>---- | | |

TECHNICAL FIELDS SEARCHED (Int. Cl.4)

H 01 L 21/00
G 01 M 11/00
G 01 N 21/00
G 01 B 9/00
G 01 B 11/00

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| VIENNA | 12-02-1986 | TOMASELLI |

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
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